CLAIMS:

1. A integrated circuit comprising:

a plurality of pairs of latches (L1, L2) being respectively clocked by two non-overlapping clock signals ($\Phi 1$, $\Phi 2$).

2. A integrated circuit as claimed in claim 1, wherein delay circuits (τ) are placed between clock inputs of latches (L) of a same clock phase ($\Phi 1$ or $\Phi 2$).

3. A integrated circuit as claimed in claim 2, wherein each delay circuit (B) drives more than one latch.